High Frequency Limitations of Active Rectifier Circuits for RFID Applications

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***Abstract*—This paper analyses the frequency limitations of an active rectifier for RFID applications that has been optimised for 13.56 MHz. The rectifier utilises an active MOS diode with threshold cancellation and a control scheme to reduce reverse leakage. The rectifier is implemented in AMS 0.35 μm CMOS and simulated in Cadence Spectre. For an input voltage of 2 V and an output current of 20 μA, a power and voltage conversion efficiency of 83 % and 89 %, respectively, are achieved at 13.56 MHz. We show that reducing the width of the main MOS transistor from 90 to 60 μm improves the upper frequency limit, but beyond 30 MHz the finite speed of the threshold cancellation control circuit limits the efficiency of the rectifier circuit.**

***Index Terms*—RFID, rectifier, frequency response, threshold cancellation, reverse leakage, CMOS**

I. Introduction

Radio frequency identification (RFID) has been expanding continuously to new areas and applications. Access control, public transport, industrial automation and tracking of materials and goods in production flow [1] [2] are just a few examples. An RFID system consists mainly of two parts: a reader unit and a transponder, also called tag. The latter can either be active or passive. Active tags have their own power supply whereas passive tags are remotely powered by the reader unit through a magnetic or electromagnetic field, depending on the frequency of the RF signal transmitted. The signal is rectified in the tag to provide the necessary DC voltage for the operation of the tag. Since the power level of the transmitted signal is relatively small, it is important to achieve a high voltage and power conversion efficiency (VCE/PCE) of the rectifier in the tag. There are several factors that influence the PCE of rectifiers. Firstly, the fixed turn-on voltage of the diodes does not only define the dead zone where the received induced AC voltage level is not sufficient to power up the tag, it also generates a power loss in the diode which is directly proportional to the conducted current. The turn-on voltage is dependent on the threshold voltage of the diode. Schottky diodes have a very low threshold compared to MOS diodes, but are only available in advanced CMOS processes which increases the costs. One cost-efficient alternative is the use of a threshold cancellation technique [3], [4], [5] to minimise the power loss in the diode and thereby increase the PCE. A more detailed description of a threshold cancellation technique follows in the next section. A second important factor which leads to a decrease in PCE is reverse leakage. Several control schemes, based on comparators, have also been investigated to minimise this problem [6], [7].

One key challenge in the use of passive tags in industrial harsh environment is the transfer of energy over long distances and to tags of unknown orientation. Previous work on RFID systems for applications in tracking production flows concentrated on the frequency band around 125 kHz. It could be beneficial to shift the frequency band to around 13.56 MHz or even higher. Even though the permissible magnetic field power is lower than on 125 kHz, but only by 6 dB (EU directive 2013/752/EU), the frequency is around a factor of 100 higher, which means the induced voltage in an antenna could, theoretically, be up to 50 times higher at 13.56 MHz. This in turn means the active diode will be turned on earlier and hence, will lead to lower loss. Another advantage that comes with higher frequencies is the fact that it allows for simpler antennas with lower inductance and thus lower number of turns.

Many publications on rectifier circuits with the aim to improve their operation at 13.56 MHz exist. However, a quantitative comparison is rather difficult as the general conditions like input voltage and output resistance vary a lot. In [6] a full wave active rectifier with 2 V input and a 500 Ω output resistance achieves a PCE of about 84 %. Another active full wave rectifier is presented in [7]. Here a PCE greater than 80 % is reported for input voltages above 2 V. A voltage doubler rectifier with 500 mV input and a 10 kΩ output resistance is presented in [8]. For this setup the rectifier achieves a PCE of 80 %. Some of these works looked briefly into the operation at frequencies above 13.56 MHz but without further investigation of frequency limitations.

In this work a MOS rectifier with threshold cancellation and a reverse leakage control scheme is investigated in terms of its frequency response and limitations for frequencies above 1 MHz. The circuit is optimised for 13.56 MHz operation and the limitations incurred as the frequency is increased are analysed. In section II the initial circuit used for the investigation is presented, including a short illustration of the applied threshold cancellation technique and the optimisation of the circuit for 13.56 MHz. The frequency response and limitations of the optimised circuit are described in section III. Various steps to increase the frequency range are investigated and the simulation results that were obtained with Cadence Spectre are presented and discussed. Conclusions follow in section IV.

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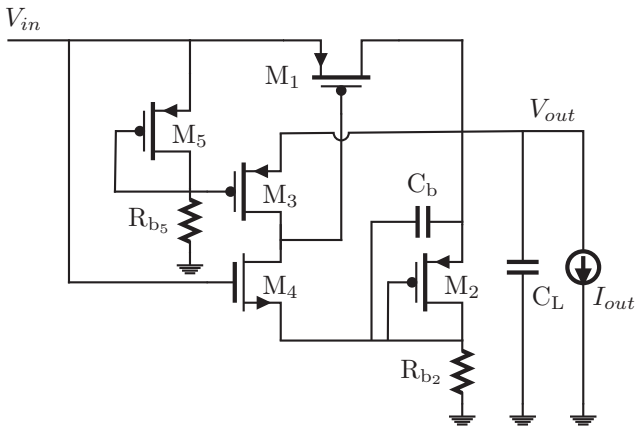


Fig. 1. Initial circuit design for single MOS diode rectifier with threshold cancellation and reverse leakage control [9].

II. Circuit Design

A. Utilised Rectifier

As a starting point served the circuit presented in [9], also shown in Fig. 1. It is based on an internal threshold cancellation technique for MOS diodes and, in addition, utilises a control scheme to minimise reverse leakage. The main idea of the threshold cancellation technique is to place a diode connected MOS transistor (M_2 in Fig. 1) between drain and gate of the MOS diode M_1 to reduce the effective threshold of it. However, the reverse leakage will increase rapidly when the transistor M_1 is reverse-biased if the effective threshold is reduced. To minimise the reverse leakage, a CMOS inverter, M_3 and M_4, is added. Its purpose is to switch between activating the threshold cancellation during the positive half-period of the input signal and turning off M_1 completely during the negative half-period. By operating M_1 as a reduced-threshold MOS diode rather than as a pure CMOS switch, the exact timing of the turn on and turn off instances becomes less critical. Thus, the need for a fast and highly accurate control circuit is reduced and a simple driver circuit as shown in Fig. 1 has been shown to be sufficient for operation at low frequencies up to 1 MHz.

In the original design, which was optimised for 1 MHz, the widths of the transistors M_1, M_2, M_3, M_4 and M_5 were chosen as follows: 200 µm, 1 µm, 5 µm, 5 µm and 1 µm, respectively. The resistor sizes R_{b2} and R_{b5} were set to 700 kΩ and 1 MΩ, respectively.

B. Optimisation for 13.56 MHz

This and all following circuits were implemented in the AMS 0.35 µm CMOS process and simulated with Cadence Spectre.

At an operating frequency of 1 MHz, the circuit with its original parameters, an input voltage of 2 V and an output current of 20 µA achieved a PCE and VCE of 84.9 % and 92.4 %, respectively. The distribution of power dissipation in selected components are shown in table I. The biggest loss contributor is M_1 with 42 % of the overall loss. With the frequency increased to 13.56 MHz the PCE and VCE dropped down to 79.2 % and 86.6 %, respectively and the power dissipation in M_1 increased to 57 % of the overall loss. Fig. 2 shows the voltage signal at the gate of M_1 as well as the current through the transistor for both operation at 1 and 13.56 MHz. In the latter case it becomes apparent that M_1 doesn't switch fast enough, so neither threshold cancellation nor leakage control are working to their full potential as the frequency increases. There are two possibilities to overcome this problem and to thereby increase efficiency; decrease the width of M_1 and increase the current that can be sunk by M_4 when turning on M_1. To achieve the latter, R_{b2} has to be decreased and M_2 scaled accordingly to keep the desired threshold cancellation voltage. This leads to a trade-off because it in turn means a higher current through the resistor and thus higher loss in power. A parametric analysis of the width of M_1 shows that decreasing the width to 90 µm results in the highest PCE at 13.56 MHz. Further parametric analyses were performed to determine the the optimum values for R_{b2} (700 kΩ) and the widths (3 µm) of the transistors (M_3 and M_4) of the inverter. With the circuit parameters changed to the optimum values, the PCE and VCE could be increased up to 82.9 % and 89.2 %, respectively, only slightly below the achieved values at an operating frequency of 1 MHz. Still M_1 remains the main contributor to the power dissipation, with 50 % of the overall loss.

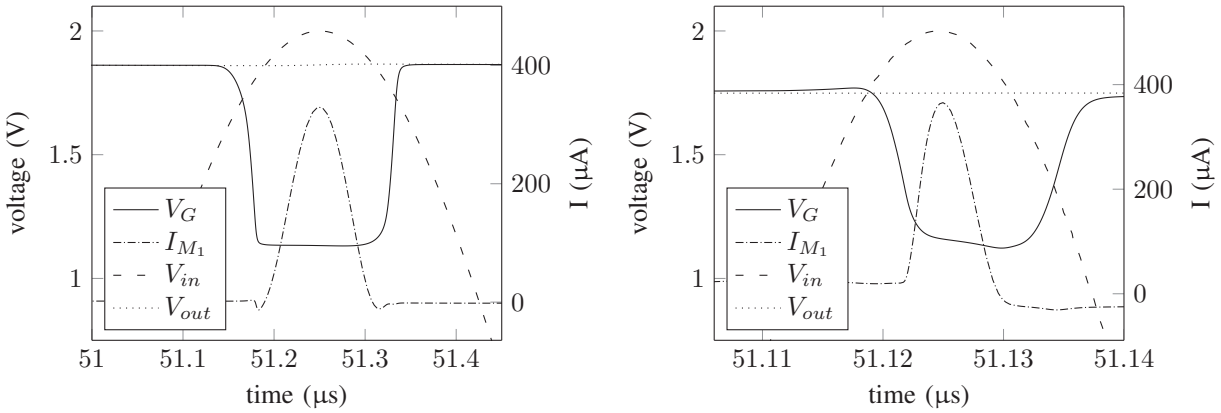
III. Frequency Limitations

To investigate the optimised circuit's frequency response and its limits, the frequency was first doubled from 13.56 MHz onwards and later some intermediate steps were added. Already at around 30 MHz the PCE and VCE started to drop significantly (Fig. 3). The power loss distribution in Table I shows, that again, M_1 is the main contributor with its power loss increased to 62 % of the overall loss at 27.12 MHz. Similarly as for the original circuit, the switching speed of M_1 is the limiting parameter. Choosing a smaller width increases the switching speed and should in turn result in better performance at higher frequency. But this comes with the cost of slightly lower PCE and VCE when operating at 13.56 MHz, where optimal performance was obtained for a width of M_1 of 90 µm. Choosing a width W_1 smaller than the optimal width found for 13.56 MHz and no other changes in the circuit's design improved the circuit's behaviour for higher frequencies. For W_1 = 60 µm the loss in PCE at 13.56 MHz compared to the width W_1 = 90 µm is negligibly small (< 0.5 %) but in turn the PCE only starts dropping significantly at around 50 MHz compared to around 30 MHz for the width W_1 = 90 µm as shown in Fig. 4.

As seen in Table I, with increasing frequency the additional power loss occurs mainly in M_1 due to the increase in reverse leakage caused by a delay in the switching time. To further investigate the source of the delayed switching and to investigate the possible upper limits of this circuit configuration, an ideal pulsed voltage source was placed at

TABLE I
DISTRIBUTION OF POWER DISSIPATION (IN μW AND PERCENTAGE OF OVERALL LOSS) IN SELECTED COMPONENTS AND POWER CONVERSION EFFICIENCY FOR DIFFERENT SETUPS AND FREQUENCIES WITH AVERAGE INPUT POWER OF 44 μW.

	original circuit		optimised circuit		pulsed V-source @M1			pulsed V-source @M3/4	
	1 MHz	13.56 MHz	13.56 MHz	27.12 MHz	13.56 MHz	27.12 MHz	216.96 MHz	13.56 MHz	27.12 MHz
PCE	84.9 %	79.2 %	82.9 %	77.0 %	83.7 %	83.3 %	78.3 %	83.4 %	77.9 %
M1	2.5 (42 %)	5.1 (57 %)	3.6 (50 %)	5.9 (62 %)	3.0 (47 %)	3.0 (47 %)	3.1 (37 %)	3.1 (47 %)	5.4 (60 %)
M3	0.5 (7 %)	0.6 (7 %)	0.5 (7 %)	0.6 (7 %)	0.4 (6 %)	0.4 (6 %)	0.5 (6 %)	0.4 (7 %)	0.5 (6 %)
M4	0.3 (5 %)	0.6 (7 %)	0.5 (7 %)	0.6 (7 %)	0.2 (3 %)	0.2 (4 %)	0.5 (6 %)	0.4 (6 %)	0.6 (6 %)
M5	0.1 (2 %)	< 0.1 (<1 %)	0.1 (1 %)	< 0.1 (<1 %)	0.1 (1 %)	< 0.1 (<1 %)	1.5 (18 %)	0.1 (2 %)	0.2 (2 %)
Rb2	1.7 (27 %)	1.9 (21 %)	1.6 (22 %)	1.7 (18 %)	1.5 (24 %)	1.5 (24 %)	2.2 (26 %)	1.6 (24 %)	1.7 (19 %)



(a) (b)

Fig. 2. Current and gate voltage of M_1 plotted together with input and output signal of the original circuit for a) 1 MHz and b) 13.56 MHz.

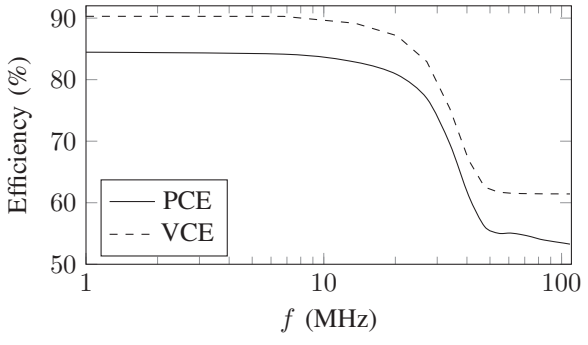


Fig. 3. PCE and VCE versus frequency for transistor width W_1 = 90 μm with $V_{in} = 2$ V and $I_{out} = 20$ μA.

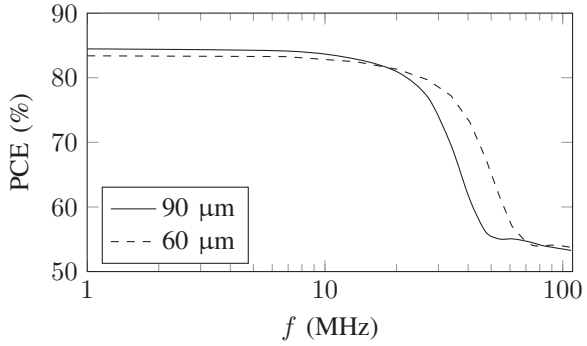


Fig. 4. Comparison of PCE for different widths of transistor M_1: optimum width (90 μm) for 13.56 MHz and a smaller width (60 μm) for improved frequency response for higher frequencies with $V_{in} = 2$ V and $I_{out} = 20$ μA.

the gate of M_1 to ensure precisely timed switching (Fig. 5). The inverter transistors M_3 and M_4 were kept to include their power dissipation in the simulations for better comparison with the simulations from the optimised circuit. With the ideal pulsed voltage source at gate M_1 the PCE could be kept above 80 % for frequencies up to 100 MHz. Even then, it only slowly decreased and was above 70 % for frequencies up to about 600 MHz. The frequency behaviour is plotted in Fig. 6. The power dissipation in M_1 only slowly increased with increasing frequency (about 10 % from 13 to 400 MHz), whereas a significant increase in power dissipation could be registered for M_5, which accounts for the main part of the additional loss for higher frequencies in this setup, as shown in Table I. Sharp signal slopes could be established with the pulsed voltage source at the gate of M_1. Both the threshold cancellation and the control scheme for minimising the reverse leakage could then work in a proper manner, resulting in high PCE and VCE and showing that the active MOS diode is well capable of operating at high frequencies.

In the next step the ideal pulsed voltage source was moved from M_1 to the inverter stage M_3/M_4. One pulsed voltage source was placed at the gate of M_3 to replace the driver circuit formed by M_5 and R_{b_5}. Again, both these components

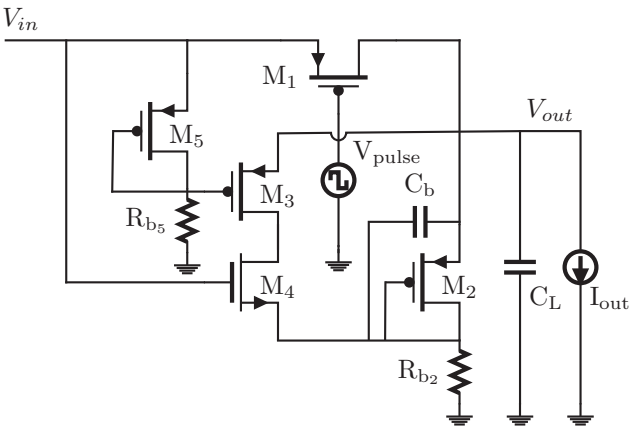


Fig. 5. Modified circuit design with pulsed voltage source at gate of M_1.

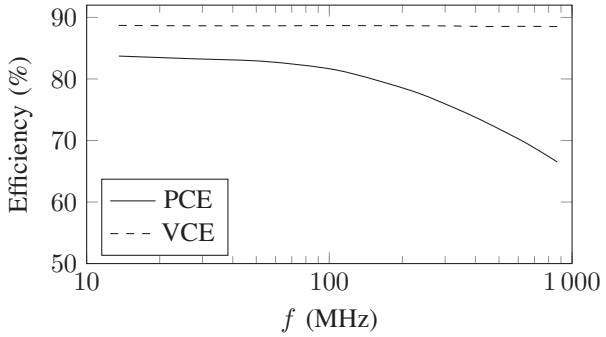


Fig. 6. PCE and VCE versus frequency for modified circuit with pulsed voltage source at gate of M_1 with $V_{in} = 2$ V and $I_{out} = 20$ µA.

were kept to include their power dissipation in the simulation for better comparison with the former simulations. Another pulsed voltage source was placed at the gate of M_4. With this setup the PCE droped below 80 % at around 25 MHz and below 70 % at around 40 MHz. Again, the main part of the loss occurred in M_1 due to M_3/M_4 not being able to drive the gate of M_1 sharply enough. Changing the widths of the inverter did not result in any improvement.

As another attempt to increase the PCE by improving the switching characteristics, two more inverter stages were added in series between the M_3/M_4 stage at the gate of M_1. The inverters were scaled with the factor e. A slight decrease in power loss in M_1 due to reduced leakage could be observed, but not enough to make up for the increased power dissipation due to the additional transistors of the additional inverter stages.

IV. Conclusion

The frequency response of an active RFID rectifier was investigated. The circuit used here utilises an active MOS diode with a threshold cancellation technique and a control scheme to minimise reverse leakage. After optimisation and slight modification, the simulations, done with Cadence Spectre in AMS 0.35 µm CMOS, showed that the rectifier is well suitable for RFID applications operating at 13.56 MHz as it reaches both high PCE (83 %) and VCE (89 %). For frequencies up to 30 MHz it still shows acceptable performance with a PCE well above 70 %. It was also shown that the active MOS diode is well capable of operating at high frequencies if sharp switching characteristics can be established at its gate. The key challenge for this lies in the steering of the signal which is generated by the preceding inverter stage.

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References

[1] B. Kvarnström, B. Bergquist, and K. Vännman. "RFID to improve traceability in continuous granular flows: An experimental case study". In: *Quality Engineering* 23.4 (2011), pp. 343–357.

[2] J. Rabe, P. Fouche, and K. O'Neill. "Development of a RF tracer for use in the mining and minerals processing industry". In: *The Third Southern African Conference on Base Metals*. 2005.

[3] H. Raben, J. Borg, and J. Johansson. "Improved efficiency in the CMOS cross-connected bridge rectifier for RFID applications". In: *Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference*. June 2011, pp. 334–339.

[4] K. Kotani and T. Ito. "High efficiency CMOS rectifier circuits for UHF RFIDs using Vth cancellation techniques". In: *ASIC, 2009. ASICON '09. IEEE 8th International Conference on*. Oct. 2009, pp. 549–552.

[5] P.T. Theilmann et al. "Near zero turn-on voltage high-efficiency UHF RFID rectifier in silicon-on-sapphire CMOS". In: *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*. May 2010, pp. 105–108.

[6] Y. Lu and W.-H. Ki. "A 13.56 MHz CMOS Active Rectifier With Switched-Offset and Compensated Biasing for Biomedical Wireless Power Transfer Systems". In: *Biomedical Circuits and Systems, IEEE Transactions on* 8.3 (June 2014), pp. 334–344.

[7] H.-M. Lee and M. Ghovanloo. "An Integrated Power-Efficient Active Rectifier With Offset-Controlled High Speed Comparators for Inductively Powered Applications". In: *Circuits and Systems I: Regular Papers, IEEE Transactions on* 58.8 (Aug. 2011), pp. 1749–1760.

[8] D. Nguyen et al. "A high power conversion efficiency rectifier with new internal VTh cancellation topology for RFID applications". In: *Communications and Electronics (ICCE), 2014 IEEE Fifth International Conference on*. July 2014, pp. 313–316.

[9] H. Raben, J. Borg, and J. Johansson. "An active MOS diode with Vth-cancellation for RFID rectifiers". In: *RFID (RFID), 2012 IEEE International Conference on*. Apr. 2012, pp. 54–57.